REMARKS

In the Official Action mailed 07 November 2007, the Examiner reviewed claims 2-15. The Examiner has objected to claims 5, 6, 9, 10 and 13 for informalities; has rejected claims 2-15 for double patenting; has rejected claims 2-15 under 35 U.S.C. §102(e); and has rejected claims 2-15 under 35 U.S.C. §102(b).

Applicant has amended claims 2, 5, 6, 9, 10, and 13, and canceled claim 3. Claims 2 and 4-15 remain pending.

Each objection and rejection is respectfully traversed below.

Objection to Claims 5, 6, 9, 10 and 13 for Informalities

The Examiner has objected to claims 5, 6, 9, 10 and 13. Such claims are amended to address the issues raised.

Accordingly, reconsideration of the objection to claims 5, 6, 9, 10 and 13 as amended is respectfully requested.

Rejection of Claims 2-15 for Double Patenting

The Examiner has rejected claims 2-15 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-54 of U.S. Patent No. 6,453,446. A terminal disclaimer will submitted to address this rejection upon indication of otherwise allowable subject matter.

Accordingly, reconsideration of the rejection of claims 2 and 4-15 as amended is respectfully requested.

Rejection of Claims 2-15 under 35 U.S.C. §102(e)

The Examiner has rejected claims 2-15 under 35 U.S.C. §102(e) as being anticipated by Tanaka *et al.* (US 5,737,237). Claim 2 is amended to incorporate the subject matter of claim 3, and claim 3 is canceled. Reconsideration is requested in view of the amendment.

Tanaka *et al.* primarily describes a placement process for functional macros, rather than for cells as required by the current claims. Accordingly, the reading of the claim language "determining initial delay values associated with the cells prior to determining an initial placement of the cells" in claim 1 on the processed in Fig. 3 and Fig. 14(a) of Tanaka *et al.* is

mistaken. Applicant submits it is not appropriate to read the claimed "cell" on a function macro as taught in Tanaka *et al.*

Fig. 3 of Tanaka *et al.* shows the basic steps of function macro placement which involves optimizing the arrangement of the function macros in light of the wiring among the function macros (See, Tanaka *et al.*, col. 8, lines 31-53). This basic process is used to optimize an "objective function." The objective function described in Tanaka *et al.* does not include cell sizing in response to placement. See, Tanaka *et al.*, col. 8, line 54 to col. 9, line 45. Rather, in relates to wiring lengths, the number of wiring lines and deviations from delay constraints for wires that interconnect function macros. Cell placement is not mentioned in connection with Fig. 3 of Tanaka *et al.*

Fig. 14(a) of Tanaka *et al.* is the first part of a process that actually places cells. However, cell placement is performed in step S26 of Fig. 14(b). Tanaka *et al.* does not discuss the claimed step of "determining an initial size or area of the cells in response to the initial placement." Tanaka *et al.* states that the leaf cells "have been prepared in the layout leaf cell library 20f" (Tanaka *et al.*, col. 15, lines 34-35), suggesting that no further sizing of the leaf cells is performed. Tanaka *et al.* does mention a "drive ability optimization process S12" in connection with Fig. 6 at col. 10, lines 33-67 (See also, step S24 in Fig. 14(a)). This process relates to changing output buffers within a function macro to meet timing constraints between function macros, after the function macro is placed but before the leaf cell corresponding to the output buffer is selected from the library.

The Office Action takes the position that the limitations in claim 3 (now in claim 2), read on the description in Tanaka *et al.* of Fig. 1(a) and Fig. 3. Fig. 3 has been discussed above. As stated above, Fig. 3 does not show cell placement. Furthermore, it does not include a step of cell sizing in response to placement. As to Fig. 1(a), a cell leaf library 10f is shown. No details of the cell leaf library 10f of Fig. 1(a) are provided by Tanaka *et al.* It is mentioned in connection with Fig. 14 (b) as described above. However, the teaching of Tanaka *et al.* in connection with the cell leaf library suggests that no sizing of cells is performed after initial placement of the cells.

Therefore, claim 2 as amended is not anticipated by nor suggested by Tanaka *et al.* Claims 4-15 depend from claim 2 as amended, and distinguish for at least the same reasons.

Without acquiescing in comments in the Office Action concerning the dependent claims not mentioned here, we note a few examples here. As to claim 4, the citations to Figs. 1(a) and 1(b) are mistaken because the processes represented relate to layout of function macros and not cell placement and sizing in response to cell placement as claimed herein.

As to claim 5, the Office Action relies upon the drive ability optimization process of Fig. 6(a), discussed above. However, the drive ability optimization of Tanaka *et al.* relates to selecting output buffers in response to function macro placement before an output buffer is selected from the leaf library. Therefore, it does not relate to sizing cells in response to an initial placement of the cells as required herein.

As to claim 6, the Office Action does not provide a citation. The conclusion stated in the Office Action is mistaken for the reasons set forth above.

Accordingly, reconsideration of the rejection of claims 2 and 4-15 as amended is respectfully requested.

Rejection of Claims 2-15 under 35 U.S.C. §102(b)

The Examiner has rejected claims 2-15 under 35 U.S.C. §102(b) as being anticipated by Frankle *et al.* (US 5,521,837). As mentioned above, claim 2 is amended to incorporate the subject matter of claim 3, and claim 3 is canceled. Reconsideration is requested in view of the amendment.

Frankle *et al.* relates to routing a functional circuit in a field programmable gate array FPGA. Cell placement as claimed herein is not relevant to this process, because the FPGA subject of Frankle *et al.* is an implemented integrated circuit. The routing being carried out by Frankle *et al.* is an attempt to optimize use of the existing routing infrastructure on the chip. See, Frankle *et al.* column 3, line 25 to column 4, line 10. Accordingly, the reliance on Frankle *et al.* is clearly mistaken. The "mapping, placing and routing" terminology in the FPGA field relate to the transferring a logic design into a hardware implementation on the FPGA using the existing gates and routing structures on the chip.

The Office Action cites Figs. 10 and 11 of Frankle *et al.* as showing the process of determining initial delay values prior to placement. However, Figs. 10 and 11 relate to iterative routing in an FPGA in which the delays being optimized relate to the path between gates on the routing infrastructure of the chip, not to cell placement and sizing as claimed herein. See, Frankle

et al., col. 12, lines 24-55; and col. 16, line 30, et seq. At the time of execution of the process of Frankle *et al*. the logic blocks, and the cells within them, on the FPGA are already implemented.

The Office Action may rely on an interpretation of the original claim 2 that is broad enough to read on the FPGA logic circuit layout process of Frankle *et al*. Applicant submits that such a broad reading is not reasonable in light of the application as a whole. Furthermore, the limitation added to claim 1, reading "determining an initial size or area of the cells in response to the initial placement" is not found in Frankle *et al*. The Office Action cites column 18, lines 40-67 and column 19 lines 1-2 as corresponding to original claim 3, from which this limitation was taken. First, there is no discussion in this passage of the size of a cell. As we have emphasized above, Frankle *et al*., including the cited passage at column 18, lines 40-67 and column 19, lines 1-2, relates to placement of logic designs on FPGA's, not to placement of cells on an integrated circuit layout and not to determining sizes of cells in such a layout.

Accordingly, reconsideration of the rejection of claims 2 and 4-15 as amended is respectfully requested.

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CONCLUSION

It is respectfully submitted that this application is now in condition for allowance (subject to the submission of a Terminal Disclaimer as mentioned above), and such action is requested.

The Commissioner is hereby authorized to charge any fee determined to be due in connection with this communication, or credit any overpayment, to our Deposit Account No. 50-0869 (SYNP 1006-0).

Respectfully submitted,

Dated: 07 May 2008 /Mark A. Haynes/

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